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PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	S. UNO, et al.
Serial No.:	09/646,671
Filed:	September 20, 2000
Title:	MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE (as amended)
Group AU:	2812
Examiner:	Lynne Ann Gurley
Confirmation No.:	2273

LETTER SUBMITTING CORRECTED FORMAL DRAWINGS

Mail Stop: ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

August 3, 2005

SIR:

Pursuant to the USPTO Supplemental Notice of Allowability, Form PTOL-37, dated May 3, 2005, attached hereto are eighty five (85) sheets of Replacement drawings. Please substitute the Replacement drawings for the corresponding drawing sheets on file in the above-identified application.

Applicants request any shortage of fees due in connection with the filing of this paper be charged to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (case 501.39082X00), and credit any excess payment of fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

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